PHILIPS

Philips Intellectual Property & Standards

FACSIMILE TRANSMITTAL TO THE UNITED STATES PATENT AND TRADEMARK OFFICE

TO:	FACSIMILE NO.:	TELEPHONE NO.:
Mail Stop Appeal Briefs-Patent Commissioner for Patents P.O. Box 1450 Arlington, VA 22313-1450	(571) 273-8300	( ) -
ATTENTION:	*Examiner:* Hong Chong KIM *Art Unit:* 2186	

FROM:		TELEPHONE NO.:
Michael J. Ure, Reg. No. 33,089		(408) 474 - 9077
RE:	*Serial No.:* 09/829,793	
	Attorney Docket No.: NL000215	

TRANSMISSION INCLUDES: 13 Pages (including cover sheet)

Transmittal of Brief In Support of An Appeal – 1 page

Appeal Brief – 11 pages

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office at the number listed above

on 11/8 2005 by _____
Daniel L. Michalek

Philips Electronics North America Corporation
1109 McKay Drive, M/S-41
San Jose, CA 95131
Tel: (408) 474-9066
Fax: (408) 474-9080

IN THE UNTED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First-Named Inventor: Martijn J. L. EMONS	Atty Docket No.: **NL000215**
Application No.: 09/829,793 Conf.: 1893	Art Unit: 2186
Date Filed: 04/10/2001	Examiner: Kim, Hong Chong
Customer No.: 24738	

Title: CACHE INTERFACE CIRCUIT FOR AUTOMATIC CONTROL OF CACHE BYPASS MODES AND ASSOCIATED POWER SAVINGS

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF
BRIEF IN SUPPORT OF AN APPEAL

Sir:

Enclosed is an original plus two copies of an Appeal Brief in the above-identified patent application.

Please charge the any and all required fees to Deposit Account No. 14-1270.

Date: 11/08/05

Respectfully submitted,
PHILIPS ELECTRONICS NORTH AMERICAN CORP.

By _____
Michael J. Ure, Reg. No. 33,089
1109 McKay Drive, M/S-41SJ
San Jose, California 95131
(408) 474-9077

CERTIFICATE OF MAILING or TRANSMISSION

I hereby certify that this correspondence is being:

☐ deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to "Commissioner for Patents, Washington, D.C. 20231",

-OR-

☒ facsimile transmitted to the USPTO, on the date indicated below.

(Date) 11/8/05 (Signature) _____

(Name) Daniel L. Michalek

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Martijn J.L. Emons**
Application No.	:	**09/829,793**
Filed	:	**April 10, 2001**
For	:	**CACHE INTERFACE CIRCUIT FOR AUTOMATIC CONTROL OF CACHE BYPASS MODES AND ASSOCIATED POWER SAVINGS**

APPEAL BRIEF

On Appeal from Group Art Unit 2186

Date: November 8, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

Certificate of Fax/Mailing Under 37 CFR 1.8

I hereby certify that this correspondence is being faxed to (703) 872-9306 or deposited with the United States Postal Service as first class mail in an envelope addressed to the COMMISSIONER FOR PATENTS, Mail Stop Appeal, P.O. BOX 1450 ALEXANDRIA, VA 22313 on November 8, 2005.

Daniel Michalek
(Name)

(Signature and Date)

TABLE OF CONTENTS

TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 6-8 are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a data processing arrangement for achieving substantial power savings.

A cache memory is used to speed processor operation. A cache memory, however, consumes significant power. The present invention provides for a cache bypass

mode, *under programmer control*, in which the cache memory is turned off, saving power. Because entry of cache bypass mode is under programmer control, the programmer can ensure that processing speed is less critical than power savings for code sections that are executed during cache bypass mode (Specification, page 2, lines 3-15).

Independent claim 6 relates to a cache interface circuit including a processor interface for receiving memory access requests from a processor, and for transmitting memory data back to the processor in response to processor requests, and a main memory interface for issuing main memory access requests to a main memory and for receiving main memory data in response. A cache memory interface is provided for issuing memory access requests to a cache memory, if operating in a cache mode, and for receiving cache memory data in response. A cache-bypass mode-control signal input for the processor is used to indicate a cache bypass mode in response to a programmer instruction inserted in a program being executed by the processor *explicitly for the purpose of switching to cache bypass mode*, in which cache bypass mode memory access requests are serviced from the main memory. A power control output is provided for switching off operating power to the cache memory in response to a command received at the cache-bypass mode-control signal input that indicates all memory access requests should be serviced from the main memory.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 6-8 are unpatentable over Fuller, or unpatentable over Fuller in view of Yamahata.

VII. ARGUMENT

I. Rejection of Claims 6-8 as Being Unpatentable over Fuller or Fuller in view of Yamahata

As noted previously, A distinguishing feature of the present invention as set forth in claim 6 is the ability of a processor to itself control whether or not the processor's cache is bypassed, enabling the cache to be switched off for power savings. Note in particular the fourth element of claim 6, reciting "a cache-bypass mode-control signal input for said processor to indicate indicate a cache bypass mode in response to a programmer instruction inserted in a program being executed by said processor explicitly for the purpose of switching to cache bypass mode."

In Fuller, by contrast, the programmer does not have any such control. Rather in Fuller, a power management unit, in response to a *fixed control program*, determines whether or not cache-bypass mode will be entered (Fuller, Fig 2; note element 65). Fuller therefore does not anticipate the present invention.

Furthermore, in Yamahata, cache-bypass mode is inferred from selected instructions as made clear in col. 2 thereof, i.e., IN or OUT instructions, STRING instructions, PRIVILEGE instructions, TASK SWITCHING instructions, or SEMAPHORE DATA operation instructions. Such a mechanism remains inflexible compared with the claimed invention.

There is no teaching or suggestion in the cited references of "a cache-bypass mode-control signal input for said processor to indicate indicate a cache bypass mode in response to a programmer instruction inserted in a program being executed by said processor explicitly for the purpose of switching to cache bypass mode."

Accordingly, claim 6 and its dependent claims are believed to patentably define over the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: November 8, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

IX. APPENDIX: THE CLAIMS ON APPEAL

6. A cache interface circuit, comprising:

a processor interface for receiving memory access requests from a processor, and for transmitting memory data back to said processor in response to processor requests;

a main memory interface for issuing main memory access requests to a main memory and for receiving main memory data in response;

a cache memory interface for issuing memory access requests to a cache memory, if operating in a cache mode, and for receiving cache memory data in response;

a cache-bypass mode-control signal input for said processor to indicate a cache bypass mode in response to a programmer instruction inserted in a program being executed by said processor explicitly for the purpose of switching to cache bypass mode, in which cache bypass mode memory access requests are serviced from said main memory;

a power control output for switching off operating power to said cache memory in response to a command received at said cache-bypass mode-control signal input that indicates all memory access requests should be serviced from said main memory.

7. The cache interface circuit of Claim 6, further comprising:

a cache-bypass mode program instruction interceptor connected to the processor interface and providing for switching between said cache and cache-bypass

modes without having received an explicit signal to do so at the cache-bypass mode-control signal input;

wherein, said processor need not take any action to switch between said cache and cache-bypass modes.

8. The cache interface circuit of Claim 7, further comprising:

a sequence of program instructions disposed in said main memory that require execution by said processor in said cache mode and that are bracketed by program instructions acted on by the cache-bypass mode program instruction interceptor to switch between said cache and cache-bypass modes.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE